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For: SEMICONDUCTOR INTEGRATED CIRCUIT DEVICE

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Arlington, VA 22202

Sir:

VERIFICATION OF A TRANSLATION

I, Kanzo Komazawa, a translator working for SANO PATENT OFFICE, having my business office at Tenmabashi-Yachiyo Bldg. Bekkan, 2-6, Tenmabashi-Kyomachi, Chuo-Ku, Osaka-Shi, Osaka 540-0032, Japan, hereby declare and say:

That I am thoroughly conversant with both the Japanese and English languages; and that the attached document represents a true English translation of Japanese Patent Application No. 2003-048369 filed in the JPO on February 26, 2003, for which priority benefits are claimed under 35 U.S.C. §119.

I further declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so

made are punishable by fine or imprisonment, or both, under §1001 of Title 18 of the United

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application or any patent issued thereon.

Signed this 7th day of July, 2006.

Signature: _____*K.Komazawa*_____

Name: Kanzo KOMAZAWA

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[Title of the Invention]   SEMICONDUCTOR INTEGRATED CIRCUIT DEVICE

[Number of Claims]   6

[Inventor]

    [Address]   c/o ROHM CO., LTD.

                21, Saiin Mizosaki-cho, Ukyo-ku,

                Kyoto-shi, Kyoto, Japan

    [Name]   YAMAMOTO Seiichi

[Inventor]

    [Address]   c/o ROHM CO., LTD.

                21, Saiin Mizosaki-cho, Ukyo-ku,

                Kyoto-shi, Kyoto, Japan

    [Name]   MAEDA Norihiro

[Inventor]

    [Address]   c/o ROHM CO., LTD.

                21, Saiin Mizosaki-cho, Ukyo-ku,

                Kyoto-shi, Kyoto, Japan

    [Name]   UEDA Toyokazu

[Applicant]

    [Identification Number]   000116024

    [Name]   ROHM CO., LTD.

[Agent]

    [Identification Number]   100085501

    [Patent Attorney]

    [Name or Corporate Name]   SANO Shizuo

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[List of the Attached Documents]

       [Title of the Document]   Specification   1 copy

       [Title of the Document]   Drawings   1 copy

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[Proof]   Required

[Title of the Document]   Specification

[Title of the Invention]   SEMICONDUCTOR INTEGRATED CIRCUIT DEVICE
[Claims]

[Claim 1]   A semiconductor integrated circuit device comprising:

a power transistor that feeds a large current to a load;

a first transistor of which a second electrode and a control electrode are connected respectively to a second electrode and a control electrode of the power transistor;

a second transistor of which one of a first electrode or a second electrode is connected to a first electrode of the first transistor; and

an operational amplifier

of which one input terminal is connected to a first electrode of the power transistor,

of which another input terminal is connected to the first electrode of the first transistor, and

of which an output terminal is connected to a control electrode of the second transistor,

wherein the second transistor outputs, at another of the first and second electrodes thereof, a current signal proportional to a current flowing through the power transistor.

[Claim 2]   A semiconductor integrated circuit device as claimed in claim 1,

wherein the second transistor and the operational amplifier constitute a negative feedback circuit.

[Claim 3]   A semiconductor integrated circuit device comprising:

a power transistor that feeds a large current to a load;

a first transistor of which a second electrode and a control electrode are connected respectively to a second electrode and a control electrode of the power transistor;

a second transistor of which a second electrode is connected to a first electrode of the first transistor; and

a third transistor of which a control electrode is connected to a first electrode of the power transistor and of which a second electrode is connected to a control

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electrode of the second transistor,

wherein the second transistor outputs, at a first electrode thereof, a current signal proportional to a current flowing through the power transistor.

[Claim 4]   A semiconductor integrated circuit device as claimed in claim 3,

wherein the second and third transistors are transistors of opposite polarities, and a potential difference appearing between the second electrode and control electrode of the second transistor is substantially equal to a potential difference appearing between the second electrode and control electrode of the third transistor.

[Claim 5]   A semiconductor integrated circuit device as claimed in claim 4,

wherein the second transistor is a transistor of a same polarity as the first transistor.

[Claim 6]   A semiconductor integrated circuit device as claimed in claims 3 to 5,

wherein a first electrode of the third transistor is connected to the second electrodes of the power transistor and the first transistor, and a direct-current voltage is applied through a resistor to the second electrode of the third transistor.

[Detailed Description of the Invention]

[0001]

[Field of the Invention]

The present invention relates to a semiconductor integrated circuit device provided with a power transistor, such as a power MOSFET or power bipolar transistor, through which a large current is passed.

[0002]

[Prior Art]

In a semiconductor integrated circuit device, such as a motor driver, that is provided with a power transistor through which a large current is passed to drive a load, there is usually provided, for the purpose of preventing the power transistor from being destroyed as a result of a current larger than the rated current flowing therethrough, a current detection circuit for detecting the current that flows through the power transistor or an overcurrent protection circuit. One type of such a current detection circuit or overcurrent protection circuit achieves current detection by the use of a resistor for current detection which is connected directly

in the circuit that includes the power transistor.

[0003]

In some applications, a semiconductor integrated circuit device provided with a power transistor is operated from a supply voltage as low as, for example, 5 V. In such a case, to secure a sufficiently wide dynamic range in the voltage fed to the load, it is necessary to minimize the voltage drop in the voltage fed to the load. Thus, considering the voltage drop across the resistor for current detection which is connected in series with the circuit including the power transistor, the circuit configuration described above is not fit for a semiconductor integrated circuit device that is operated from a low supply voltage.

[0004]

As examples of prior-art techniques that employ a current detection circuit or overcurrent protection circuit in which the aforementioned voltage drop is reduced, there are proposed power MOSFETs furnished with an overcurrent protection function wherein the power transistor is protected from overcurrent according to the current from a transistor whose drain and gate are kept at the same potentials as the drain and gate, respectively, of the power transistor (see Patent Publications 1 to 5). As another example of a prior-art technique, there is proposed a semiconductor device wherein a power FET and a sense FET connected in parallel with the power FET are connected individually to the input terminals of an operational amplifier so that current detection is achieved by monitoring the potential difference between the output terminal of the operational amplifier and the input terminal of the sense FET (see Patent Publication 6).

[0005]

[Patent Publication 1]
Japanese Patent Applications Published No. H7-120221
[Patent Publication 2]
Japanese Patent Applications Published No. H8-34222
[Patent Publication 3]
Japanese Patent Applications Laid-Open No. 2002-16219
[Patent Publication 4]
Japanese Patent Applications Laid-Open No. 2002-26707
[Patent Publication 5]

Japanese Patent Applications Laid-Open No. 2002-280886

[Patent Publication 6]

Japanese Patent Application Laid-Open No. H6-61432

[0006]

[Problems to be Solved by the Invention]

In an overcurrent protection circuit or current detection circuit configured as proposed in Patent Publication 1 to 5, the current through the power transistor is detected by detecting the current from the transistor whose drain and gate are kept at the same potentials as the drain and gate, respectively, of the power transistor. However, in this configuration, the sources of the two transistors are not forcibly kept at the same potential. Accordingly, the transistor for current detection and the power transistor do not operate in the perfectly identical state. Thus, it is not always possible to detect a current proportional to the current that flows through the power transistor.

[0007]

On the other hand, in the semiconductor device proposed in Patent Publication 6, a resistor is connected between the inverting input terminal and output terminal of the operational amplifier, and therefore, even when the source current of the sense FET is outputted as a detection current from the inverting input terminal side of the operational amplifier, part of the source current of the sense FET flows through the resistor into the operational amplifier. Thus, the source current of the sense FET is not completely outputted, but varies according to the state in which it is operating. This necessitates adopting a configuration in which the current though the power FET is detected by detecting the difference between the voltage on the output terminal side of the operational amplifier and the voltage on the inverting input terminal side of the operational amplifier.

[0008]

Furthermore, in this configuration, to pass the source current of the sense FET through the resistor connected between the output terminal and inverting input terminal of the operational amplifier, the inverting input terminal of the operational amplifier needs to be connected to a circuit stage into which no current flows from an input terminal of a comparator, operational amplifier, or the like. That is, it is necessary to provide a circuit functioning as a voltage

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amplification stage in the succeeding stage. Moreover, to output a current signal, this voltage amplification stage needs to be built as a voltage-to-current conversion stage.

[0009]

An object of the present invention is to provide a semiconductor integrated circuit device that permits a transistor used for current detection to operate in the identical state with a power transistor and that outputs a current signal as a detection signal.

[0010]

[Means for Solving the Problem]

To achieve the above object, a semiconductor integrated circuit device as claimed in claim 1 is provided with: a power transistor that feeds a large current to a load; a first transistor of which the second electrode and the control electrode are connected to the second electrode and the control electrode of the power transistor; a second transistor of which one of the first electrode and the second electrode is connected to the first electrode of the first transistor; and an operational amplifier of which one input terminal is connected to the first electrode of the power transistor, of which the other input terminal is connected to the first electrode of the first transistor, and of which the output terminal is connected to the control electrode of the second transistor. Here, the second transistor outputs, at the other of the first and second electrodes thereof, a current signal proportional to the current flowing through the power transistor.

[0011]

With this configuration, since the voltages at both of the input terminals of the operational amplifier are approximately equal, the voltages applied to the first electrodes of the power transistor and the first transistor are approximately equal, and this permits the power transistor to operate in substantially the identical state with the first transistor. Hence, when the power transistor and the first transistor are MOSFETs, a current proportional to their (Gate Width) / (Gate Length), or when the power transistor and the first transistor are bipolar transistors, a current proportional to their emitter areas, is outputted as a detection current signal, and thus the current flowing through the power transistor is detected.

[0012]

Alternatively, as claimed in claim 2, the second transistor and the operational amplifier constitute a negative feedback circuit. In this configuration, when the second transistor is an N-channel MOSFET or an npn-type bipolar transistor, the connection node between the first and second transistors is connected to the inverting input terminal of the operational amplifier. When the second transistor is a P-channel MOSFET or a pnp-type bipolar transistor, the connection node between the first and second transistors is connected to the non-inverting input terminal of the operational amplifier.

[0013]

A semiconductor integrated circuit device as claimed in claim 3 is provided with: a power transistor that feeds a large current to a load; a first transistor of which the second electrode and the control electrode are connected to the second electrode and the control electrode of the power transistor; a second transistor of which the second electrode is connected to the first electrode of the first transistor; and a third transistor of which the control electrode is connected to the first electrode of the power transistor and of which the second electrode is connected to the control electrode of the second transistor. Here, the second transistor outputs, at the first electrode thereof, a current signal proportional to the current flowing through the power transistor.

[0014]

With this configuration, as claimed in claim 4, the second and third transistors are transistors of opposite polarities, and the potential difference appearing between the second electrode and control electrode of the second transistor is substantially equal to the potential difference appearing between the second electrode and control electrode of the third transistor. This makes it possible to apply approximately equal voltages to the first electrodes of the power transistor and the first transistor.

[0015]

Hence, when the power transistor and the first transistor are MOSFETs, a current proportional to their (Gate Width) / (Gate Length), or when the power transistor and the first transistor are bipolar transistors, a current proportional to their emitter areas, is outputted as a detection current signal, and thus the current flowing through the power transistor is detected. In this configuration, when the

second and the third transistors are MOSFETs, their source-gate voltages, or when the second and the third transistors are bipolar transistors, their base-emitter voltages, are set to be substantially equal.

[0016]

Alternatively, as claimed in claim 5, the second transistor is a transistor of the same polarity as the first transistor. That is, when the first transistor is an N-channel MOSFET or an npn-type bipolar transistor, the second transistor is an N-channel MOSFET and the third transistor is a P-channel MOSFET, or alternatively, the second transistor is an npn-type bipolar transistor and the third transistor is a pnp-type bipolar transistor; when the first transistor is a P-channel MOSFET or a pnp-type bipolar transistor, the second transistor is a P-channel MOSFET and the third transistor is an N-channel MOSFET, or alternatively, the second transistor is a pnp-type bipolar transistor and the third transistor is an npn-type bipolar transistor.

[0017]

Furthermore, as claimed in claim 6, the first electrode of the third transistor is connected to the second electrodes of the power transistor and the first transistor, and a direct-current voltage is applied through the resistor to the second electrode of the third transistor.

[0018]

[Embodiment]

First Embodiment

A first embodiment of the present invention will be described below with reference to the drawings. Fig. 1 is a circuit block diagram showing an example of the internal configuration of the semiconductor integrated circuit device provided with a power transistor according to this embodiment.

[0019]

The semiconductor integrated circuit device shown in Fig. 1 is composed of: a power transistor M1 that feeds a current to a load L; a transistor M2 of which the gate and source are connected to the gate and source, respectively, of the power transistor M1; an operational amplifier A of which the non-inverting input terminal is connected to the drain of the power transistor M1 and of which the inverting input terminal is connected to the drain of the transistor M2; and a transistor M3 of

which the gate is connected to the output terminal of the operational amplifier A and of which the source is connected to the drain of the transistor M2.

[0020]

The sources of the power transistor M1 and the transistor M2 are grounded via a ground terminal 10, and a control signal is fed via a control terminal 11 to the gates of the power transistor M1 and the transistor M2. The drain of the power transistor M1 is connected via a load terminal 12 to a load L. The drain of the transistor M3 is connected to a detection terminal 13 via which a detection current is fed out. Here, the power transistor M1 and the transistors M2 and M3 are all N-channel MOSFETs. The transistor M3 and the operational amplifier A constitute a negative feedback circuit.

[0021]

In the semiconductor integrated circuit device configured as described above, the voltages at the inverting and non-inverting input terminals of the operational amplifier A are approximately equal, and thus the voltages at the drains of the power transistor M1 and the transistor M2 are approximately equal. As a result, since the power transistor M1 and the transistor M2 have their sources connected together and have their gates connected together, the voltages at their drains are equal, the voltages at their sources are equal, and the voltage at their gates are equal.

[0022]

By making the voltages applied to the different electrodes of the power transistor M1 equal to the voltages applied to the corresponding electrodes of the transistor M2 in this way, the drain current through the transistor M2 can be made proportional to the drain current through the power transistor M1. Specifically, let the gate width and gate length of the power transistor M1 be W1 and L1, respectively, and let the gate width and gate length of the transistor M2 be W2 and L2, respectively. Then, with respect to the drain current I1 through the power transistor M1, the drain current I2 through the M2 is given as I1 × (W2 / L2) / (W1 / L1). Here, whereas the drain current through the transistor M2 is of the order of several μA to several ten μA, the drain current through the power transistor M1 is of the order of several hundred μA.

[0023]

Moreover, the provision of the transistor M3 permits the output voltage of

the operational amplifier A to be used for the sole purpose of being sampled as the gate voltage of the transistor M3. This helps to prevent a current from flowing out of the operational amplifier A as part of the drain current of the transistor M3, or part of the current flowing through the detection terminal 13 from flowing into the operational amplifier A, as opposed to in a case where the transistor M2 is connected through a resistor or the like directly to the output terminal of the operational amplifier A. As a result, the current appearing at the detection terminal 13 is not influenced by a current flowing into or out of the operational amplifier A, and thus the current appearing at the detection terminal 13 represents the drain current of the transistor M2, which is proportional to the drain current of the power transistor M1.

[0024]

In Fig. 1, an N-channel MOSFET is used as the transistor M3. It is, however, also possible to use, as shown in Fig. 2, an npn-type bipolar transistor as a transistor T3 in place of the transistor M3. In this case, the transistor T3 has its collector connected to the detection terminal 13, has its base connected to the output terminal of the operational amplifier A, and has its emitter connected to the drain of the transistor M2. That is, the transistor T3 and the operational amplifier A constitute a negative feedback circuit. Since the base current of this transistor T3 is negligible as compared with its collector current, just as in the case shown in Fig. 1, the current appearing at the detection terminal 13 represents the drain current of the transistor M2, which is proportional to the drain current of the power transistor M1.

[0025]

In Figs. 1 and 2, an N-channel MOSFET is used as the power transistor M1. It is, however, also possible to use, as shown in Figs. 3(a) and 3(b), an npn-type bipolar transistor as a power transistor T1 in place of the power transistor M1. In this case, in place of the transistor M2, which is an N-channel MOSFET, an npn-type bipolar transistor is used as a transistor T2.

[0026]

The non-inverting and inverting input terminals of the operational amplifier A are connected to the collectors of the power transistor T1 and the transistor T2, respectively. The emitters of the power transistor T1 and the transistor T2 are

connected to the ground terminal 10, and the bases of the power transistor T1 and the transistor T2 are connected to the control terminal 11. Fig. 3(a) shows a case where an N-channel MOSFET is used as the transistor M3, and Fig. 3(b) shows a case where an npn-type bipolar transistor is used as the transistor T3.

[0027]

In the configurations shown in Figs. 3(a) and 3(b), the operational amplifier A and the transistor M3 or T3 have the same functions as the operational amplifier A and the transistor M3 or T3 in Figs. 1 and 2. Moreover, the voltages at the emitters of the power transistor T1 and the transistor T2 are equal, the voltages at their collectors are equal, and the voltages at their bases are equal. Thus, through the power transistor T1 and the transistor T2 flow collector currents that are proportional to their emitter areas. As a result, let the emitter areas of the power transistor T1 and the transistor T2 be S1 and S2, respectively, then, with respect to the collector current I1 of the power transistor T1, the collector current I2 through the transistor T2 is I1 × S2 / S1, and this collector current I2 appears at the detection terminal 13.

[0028]

In Figs. 1, 2, 3(a), and 3(b), the power transistor M1 or T1 is connected to the non-inverting input terminal of the operational amplifier A and the transistor M2 or T2 is connected to the inverting input terminal of the operational amplifier A. It is, however, also possible to reverse the connection to the non-inverting and inverting input terminals of the operational amplifier A. Specifically, in that case, as shown in Figs. 4(a) and 4(b), the drains of the power transistor M1 and the transistor M2 are connected to the inverting and non-inverting input terminals, respectively, of the operational amplifier A, or, as shown in Figs. 4(c) and 4(d), the collectors of the power transistor T1 and the transistor T2 are connected to the inverting and non-inverting input terminals, respectively, of the operational amplifier A.

[0029]

In this case, the transistor M3 or T3 connected to the output terminal of the operational amplifier A is a P-channel MOSFET or pnp-type bipolar transistor, respectively, so that the operational amplifier A and the transistor M3 or T3 constitute a negative feedback circuit. Specifically, as shown in Figs. 4(a) and 4(c), the transistor M3 has its gate connected to the output terminal of the operational

amplifier A, has its source connected to the detection terminal 13, and has its drain connected to the non-inverting input terminal of the operational amplifier A; or, as shown in Figs. 4(b) and 4(d), the transistor T3 has its base connected to the output terminal of the operational amplifier A, has its emitter connected to the detection terminal 13, and has its collector connected to the non-inverting input terminal of the operational amplifier A.

[0030]

In Figs. 1, 2, 3(a), 3(b), and 4(a)A to 4(d), the power transistor M1 and the transistor M2 are N-channel MOSFETs, or the power transistor T1 and the transistor T2 are npn-type bipolar transistors. It is, however, also possible to use, as shown in Figs. 5(a) to 5(d), P-channel MOSFETs as the power transistor M1 and the transistor M2, or pnp-type bipolar transistors as the power transistor T1 and the transistor T2.

[0031]

In this case, as shown in Figs. 5(a) and 5(b), the drains of the power transistor M1 and the transistor M2 are connected to the non-inverting and inverting input terminals, respectively, of the operational amplifier A. Moreover, a P-channel MOSFET or pnp-type bipolar transistor is used as the transistor M3 or T3, respectively, and the non-inverting input terminal of the operational amplifier A is connected to the output terminal 12. Thus, the circuit configurations shown in Figs. 5(a) and 5(b) have, though with the opposite polarity, the same interconnection as those shown in Figs. 1 and 2.

[0032]

Alternatively, as shown in Figs. 5(c) and 5(d), the collectors of the power transistor T1 and the transistor T2 are connected to the non-inverting and inverting input terminals, respectively, of the operational amplifier A. Moreover, a P-channel MOSFET or pnp-type bipolar transistor is used as the transistor M3 or T3, respectively, and the non-inverting input terminal of the operational amplifier A is connected to the output terminal 12. Thus, the circuit configurations shown in Figs. 5(c) and 5(d) have, though with the opposite polarity, the same interconnection as those shown in Figs. 3(a) and 3(b).

[0033]

Alternatively, as shown in Figs. 6(a) and 6(b), the drains of the power

transistor M1 and the transistor M2 are connected to the inverting and non-inverting input terminals, respectively, of the operational amplifier A. Moreover, an N-channel MOSFET or npn-type bipolar transistor is used as the transistor M3 or T3, respectively, and the inverting input terminal of the operational amplifier A is connected to the output terminal 12. Thus, the circuit configurations shown in Figs. 6(a) and 6(b) have, though with the opposite polarity, the same interconnection as those shown in Figs. 4(a) and 4(b).

[0034]

Alternatively, as shown in Figs. 6(c) and 6(d), the collectors of the power transistor T1 and the transistor T2 are connected to the inverting and non-inverting input terminals, respectively, of the operational amplifier A. Moreover, an N-channel MOSFET or npn-type bipolar transistor is used as the transistor M3 or T3, respectively, and the inverting input terminal of the operational amplifier A is connected to the output terminal 12. Thus, the circuit configurations shown in Figs. 6(c) and 6(d) have, though with the opposite polarity, the same interconnection as those shown in Figs. 4(c) and 4(d).

[0035]

Second Embodiment

A second embodiment of the present invention will be described below with reference to the drawings. Fig. 7 is a circuit block diagram showing an example of the internal configuration of the semiconductor integrated circuit device provided with a power transistor according to this embodiment. In Fig. 7, such circuit elements as are found also in Fig. 1 are identified with the same reference numerals, and their detailed explanations will not be repeated.

[0036]

The semiconductor integrated circuit device shown in Fig. 7 differs from that shown in Fig. 1 in that the operational amplifier A shown in Fig. 1 is omitted, and that there are instead provided a resistor R and a transistor M4. A supply voltage VDD is fed to one end of the resistor R. The transistor M4 has its source connected to the other end of the resistor R and to the gate of the transistor M3, and has its gate connected to the drain of the power transistor M1. This transistor M4 is a P-channel MOSFET, and has its drain grounded via the ground terminal 10.

The transistors M3 and M4 have substantially equal source-gate threshold voltages Vth.

[0037]

In this configuration, if the drain voltage of the power transistor M1 is assumed to be Va, the drain voltage Va of this power transistor M1 is fed to the gate of the transistor M4, and thus the source voltage of the transistor M4 equals Va + Vth. The source voltage Va + Vth of this transistor M4 is fed to the gate of the transistor M3, and thus the source voltage of the transistor M3 equals Va + Vth − Vth = Va. This makes the drain voltage of the transistor M2 equal to Va, i.e., equal to the drain voltage of the power transistor M1.

[0038]

Accordingly, the drain voltage, gate voltage, and source voltage of the transistor M2 equal the drain voltage, gate voltage, and source voltage, respectively, of the power transistor M1. Thus, the drain current of the transistor M2 is proportional, by a factor of (Gate Width) / (Gate Length), to the drain current of the power transistor M1. Moreover, the drain voltage of the power transistor M1 is used for the sole purpose of being sampled as the gate voltage of the transistor M4, and the source voltage of the transistor M4 is used for the sole purpose of being sampled as the gate voltage of the transistor M3. This helps to reduce the influence on the drain current of the transistor M2 which is fed out via the detection terminal 13.

[0039]

Specifically, the drain current of the transistor M3 is not increased or decreased by the current that flows through the circuit constituted by the transistor M4 and the resistor R, but is equal to the drain current of the transistor M2. Moreover, the current that flows through the power transistor M1 is not increased or decreased by the current that flows through the circuit constituted by the transistor M4 and the resistor R, but is equal to the current that flows through the load L. Thus, as in the first embodiment, the current that appears at the detection terminal 13 is equal to the drain current of the transistor M2, which is proportional to the drain current of the power transistor M1.

[0040]

In Fig. 7, an N-channel MOSFET is used as the transistor M3 and a P-

channel MOSFET is used as the transistor M4. It is, however, also possible to use, as shown in Fig. 8, an npn-type bipolar transistor as a transistor T3 in place of the transistor M3 and an pnp-type bipolar transistor T4 in place of the transistor M4.

[0041]

In this case, the transistor T3 has its collector connected to the detection terminal 13, has its base connected to the other end of the resistor R, and has its emitter connected to the drain of the transistor M2. Moreover, the transistor T4 has its collector connected to the ground terminal 10, has its base connected to the drain of the power transistor M1, and has its emitter connected to the base of the transistor T3. The base currents of these transistors T3 and T4 are negligible as compared with their collector currents, and therefore, as in the case shown in Fig. 7, the current appearing at the detection terminal 13 represents the drain current of the transistor M2, which is proportional to the drain current of the power transistor M1.

[0042]

In Figs. 7 and 8, an N-channel MOSFET is used as the power transistor M1. It is, however, also possible to use, as shown in Figs. 9(a) and 9(b), an npn-type bipolar transistor as a power transistor T1 in place of the power transistor M1. In this case, in place of the transistor M2, which is an N-channel MOSFET, an npn-type bipolar transistor is used as a transistor T2.

[0043]

In Fig. 9(a), the collector of the power transistor T1 is connected to the gate of the transistor M4, and the collector of the transistor T2 is connected to the source of the transistor M3. In Fig. 9(b), the collector of the power transistor T1 is connected to the base of the transistor T4, and the collector of the transistor T2 is connected to the emitter of the transistor T3. Moreover, in Figs. 9(a) and 9(b), the emitters of the power transistor T1 and the transistor T2 are connected to the ground terminal 10, and the bases of the power transistor T1 and the transistor T2 are connected to the control terminal 11.

[0044]

In Figs. 7, 8, 9(a), and 9(b), N-channel MOSFETs are used as the power transistor M1 and the transistor M2, or npn-type bipolar transistors are used as the power transistor T1 and the transistor T2. It is, however, also possible to use P-

channel MOSFETs as the power transistor M1 and the transistor M2, or pnp-type bipolar transistors as the power transistor T1 and the transistor T2.

[0045]

Alternatively, as shown in Figs. 10(a) and 10(c), a P-channel MOSFET is used as the transistor M3, which has its source connected to the drain of the transistor M2 or to the collector of the transistor T2, and an N-channel MOSFET is used as the transistor M4, which has its gate connected to the drain of the power transistor M1 or to the collector of the power transistor T1. Thus, the circuit configurations shown in Figs. 10(a) and 10(c) have, though with the opposite polarity, the same interconnection as those shown in Figs. 7 and 9(a).

[0046]

Alternatively, as shown in Figs. 10(b) and 10(d), a pnp-type bipolar transistor is used as the transistor T3, which has its emitter connected to the drain of the transistor M2 or to the collector of the transistor T2, and an npn-type bipolar transistor is used as the transistor T4, which has its base connected to the drain of the power transistor M1 or to the collector of the power transistor T1. Thus, the circuit configurations shown in Figs. 10(b) and 10(d) have, though with the opposite polarity, the same interconnection as those shown in Figs. 8 and 9(b).

[0047]

[Advantages of the Invention]

According to the present invention, a current that flows through a first transistor, which receives at its first, second, and control electrodes voltages that are substantially equal to the voltages at the first, second, and control electrodes, respectively, of a power transistor, is outputted as a current signal. This makes the current signal that flows through the first transistor, which operates in substantially the identical state with the power transistor, proportional to the current signal that flows through the power transistor, permitting more accurate monitoring of the current that flows through the power transistor. Moreover, the current signal that flows through the first transistor and that is eventually outputted is not influenced by a current that flows through another circuit portion. This gives the outputted current signal higher reliability.

[Brief Description of the Drawings]

[Fig. 1]   A circuit block diagram showing an example of the internal configuration of the semiconductor integrated circuit device of a first embodiment of the invention.

[Fig. 2]   A circuit block diagram showing another example of the internal configuration of the semiconductor integrated circuit device of the first embodiment of the invention.

[Fig. 3]   Circuit block diagrams showing other examples of the internal configuration of the semiconductor integrated circuit device of the first embodiment of the invention.

[Fig. 4]   Circuit block diagrams showing other examples of the internal configuration of the semiconductor integrated circuit device of the first embodiment of the invention.

[Fig. 5]   Circuit block diagrams showing other examples of the internal configuration of the semiconductor integrated circuit device of the first embodiment of the invention.

[Fig. 6]   Circuit block diagrams showing other examples of the internal configuration of the semiconductor integrated circuit device of the first embodiment of the invention.

[Fig. 7]   A circuit block diagram showing an example of the internal configuration of the semiconductor integrated circuit device of a second embodiment of the invention.

[Fig. 8]   A circuit block diagram showing another example of the internal configuration of the semiconductor integrated circuit device of the second embodiment of the invention.

[Fig. 9]   Circuit block diagrams showing other examples of the internal configuration of the semiconductor integrated circuit device of the second embodiment of the invention.

[Fig. 10]   Circuit block diagrams showing other examples of the internal configuration of the semiconductor integrated circuit device of the second embodiment of the invention.

[Description of the Reference Designations]

M1, T1   power transistor

M2~M4, T2~T4   transistor

A   operational amplifier

L   load

R   resistor

[Title of the Document]   Drawings

Fig. 1
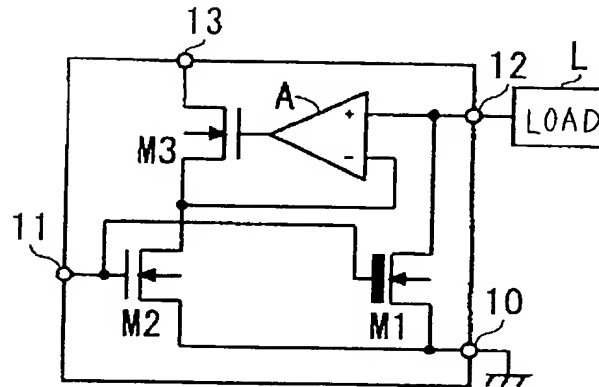
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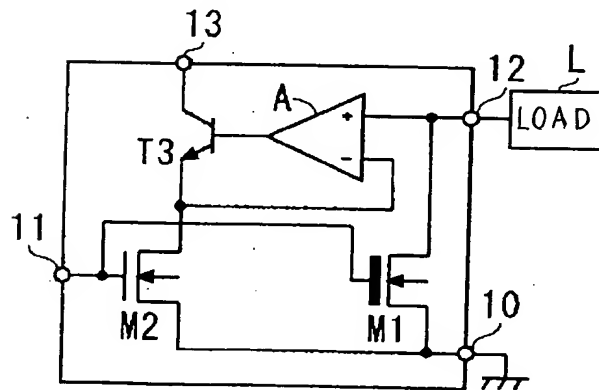
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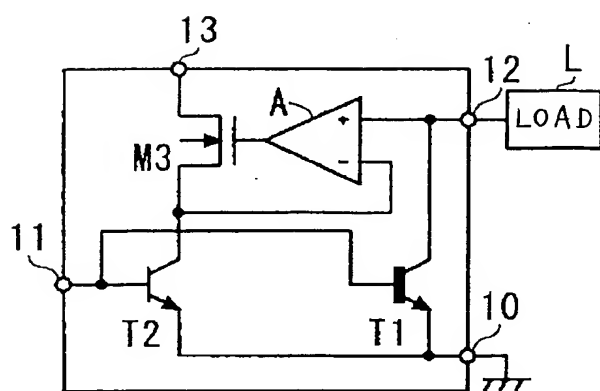
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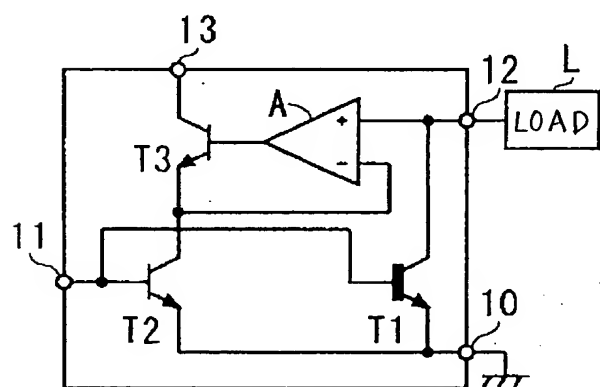
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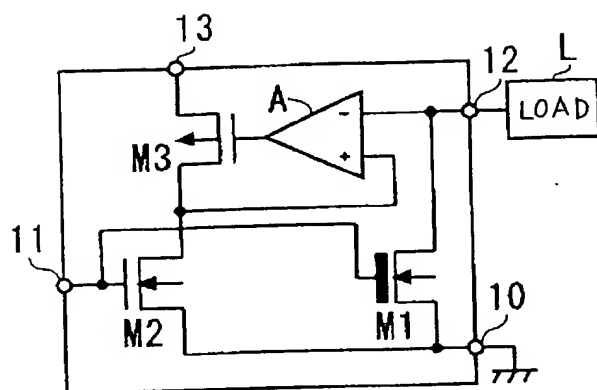
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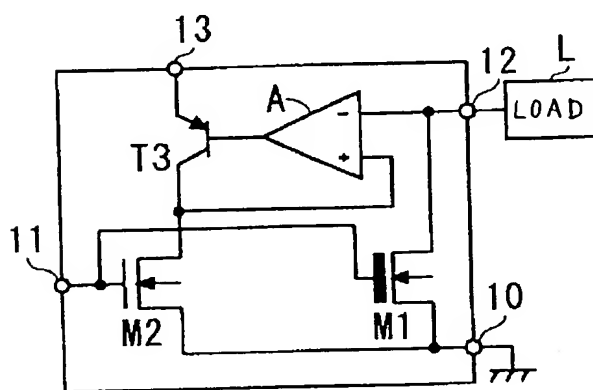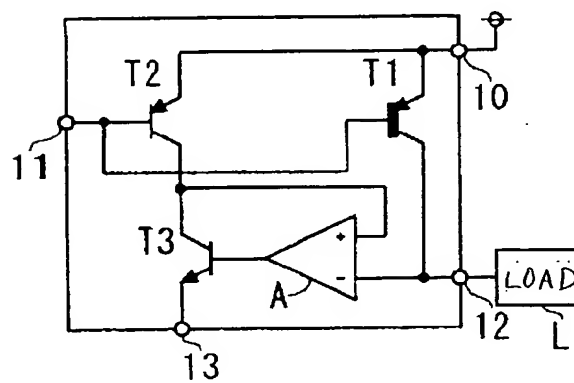
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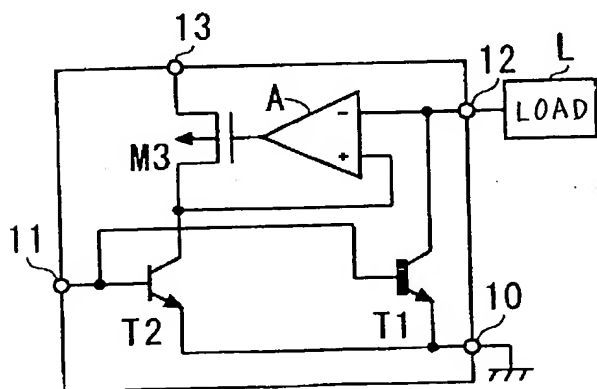
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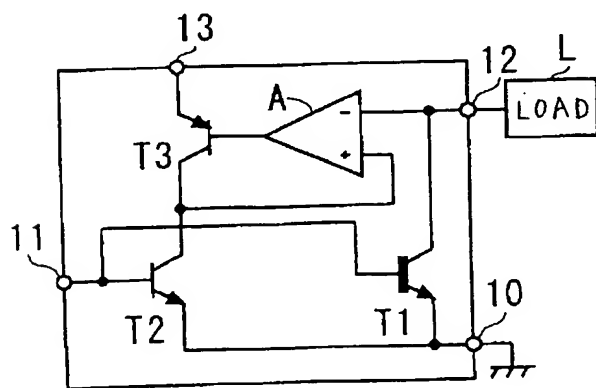
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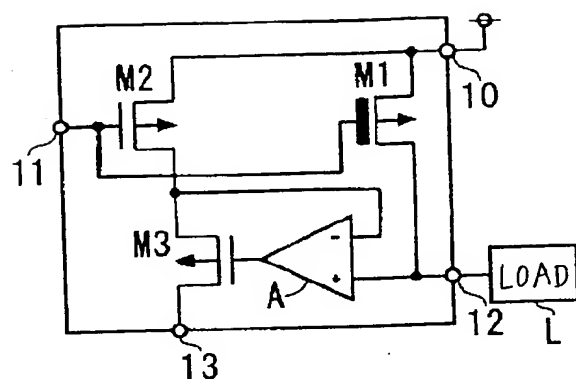
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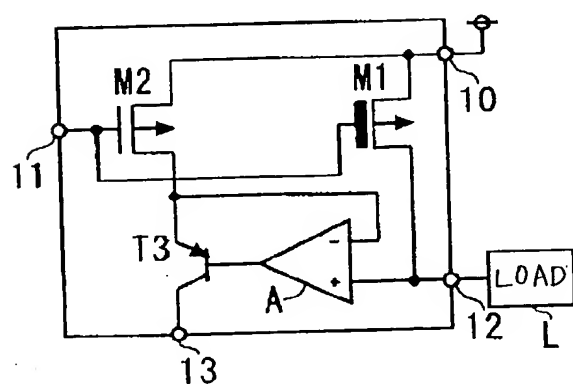
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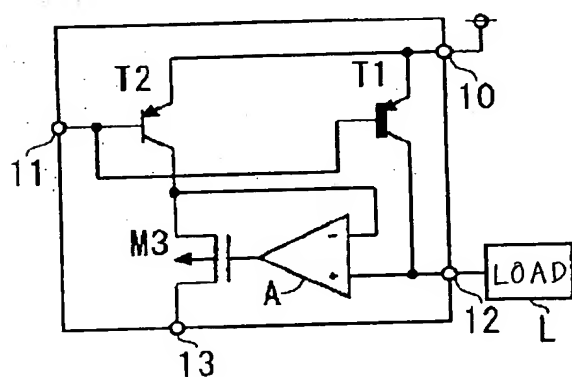
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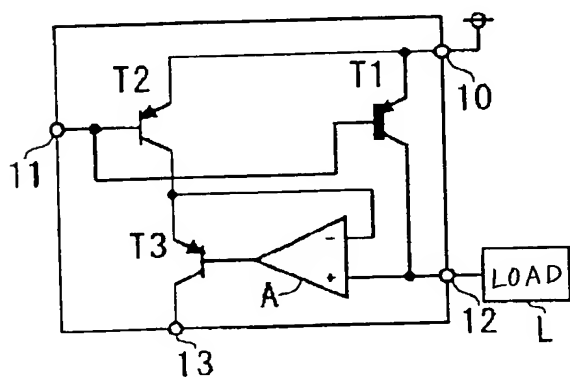
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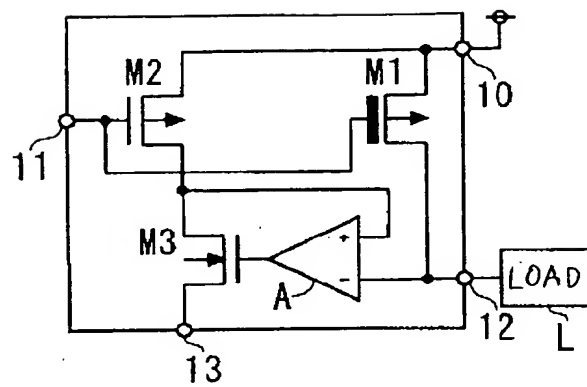
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(b)

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(d)

Fig. 7

Fig. 8

Fig. 9

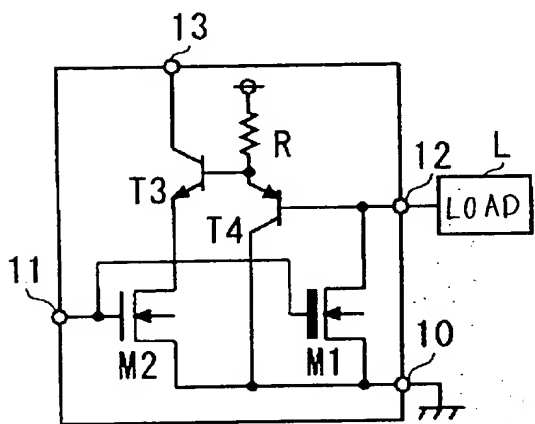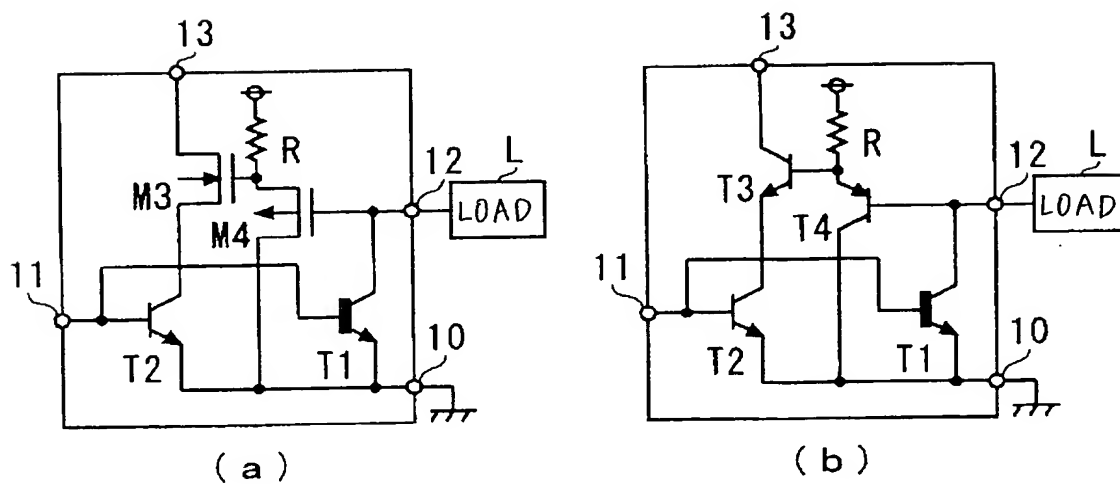(a)   (b)
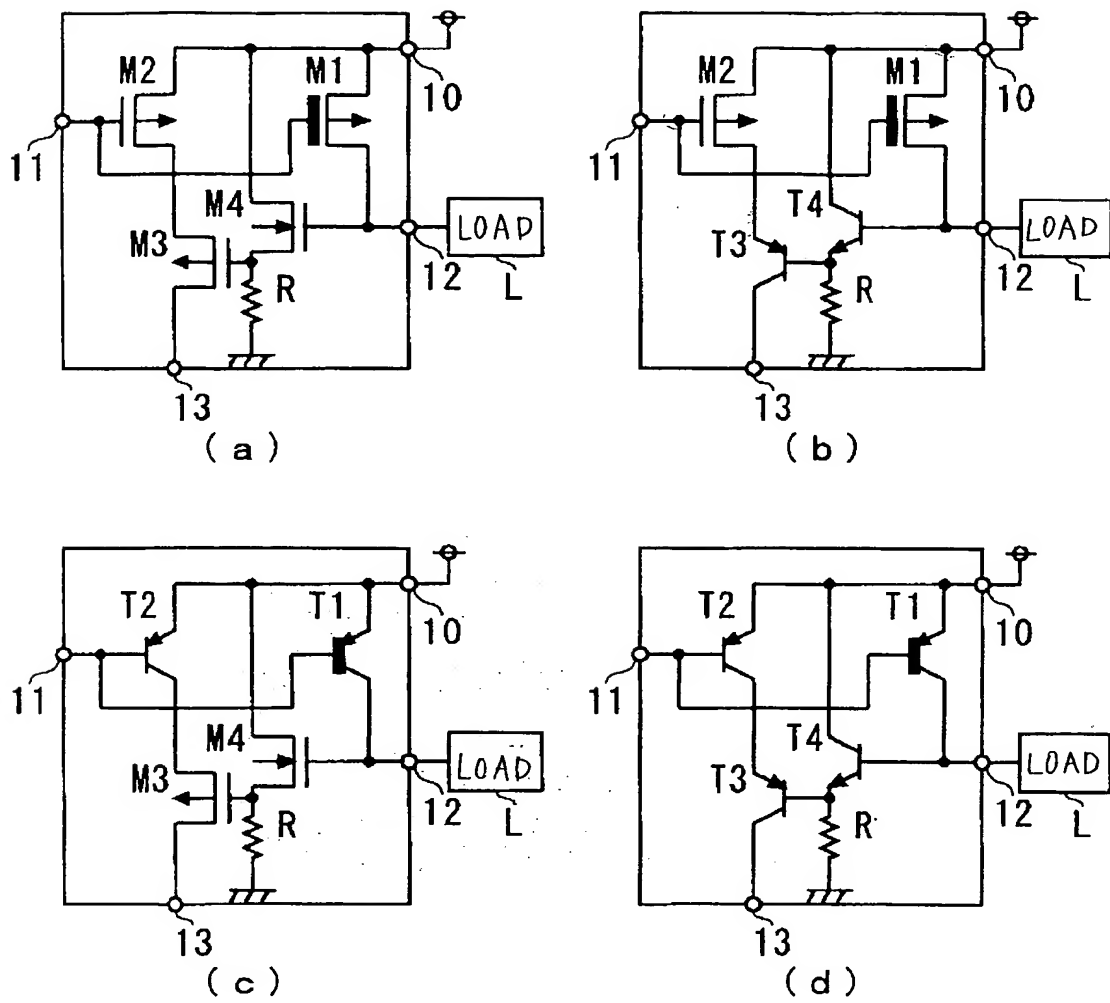
Fig. 10

（a）

（b）

（c）

（d）
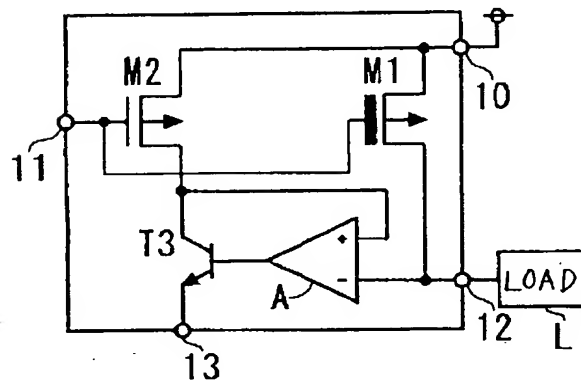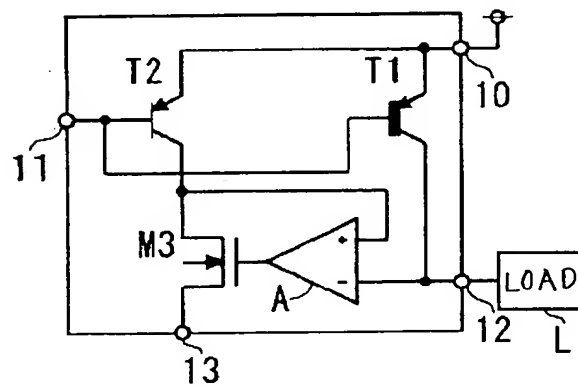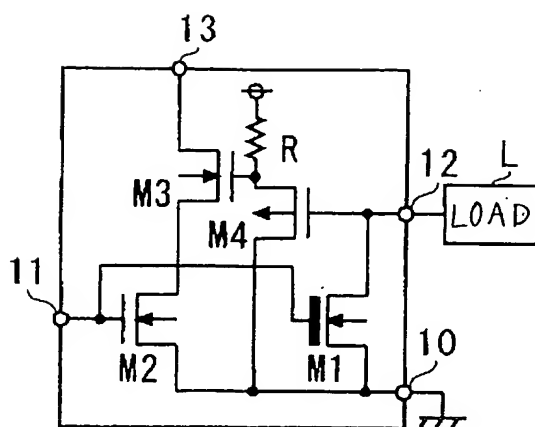
[Title of the Document]   Abstract

[Abstract]

[Object]   To provide a semiconductor integrated circuit device that permits a transistor used for current detection to operate in the identical state with a power transistor and that outputs a current signal as a detection signal.

[Features]   The non-inverting input terminal of an operational amplifier A is connected to the drain of a power transistor M1 and the inverting input terminal of the operational amplifier A is connected to the drain of a transistor M2, so that the power transistor M1 and the transistor M2, having their sources connected together and having their gates connected together, have approximately equal drain voltages.   As a result, the drain current of the transistor M2 is outputted from a detection terminal 13 as a current signal proportional to the drain current of the power transistor M1.

[Selected Figure]   Fig. 1